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EXAMINER	
LI, AIMEE J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 07/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/802,291	Applicant(s) SAULSBURY, ASHLEY
	Examiner Aimee J. Li	Art Unit 2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 8-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 8-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *24 January 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-5 and 8-22 have been considered. Claims 1, 12, and 17 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: IDS as received on 24 January 2005 and Amendment as received on 15 April 2005.

Notes on Possible Non-Compliance on Amendment

3. The Examiner would like to note that in amended claims 1 and 12 the letter "s" appeared to have strikethroughs to indicate deletion of that character, but it was not easily visible and it was not certain whether there was really a strikethrough or an image error. The Examiner believes there are strikethroughs present, since the claim would not be grammatically correct otherwise. The Examiner would like to advise Applicant that, in the future, double brackets should be used to signify strikethroughs with five or fewer characters, especially when the strikethroughs are hard to see, as is in this case with the letter "s". Should a similar situation be found in future amendments, the amendment can be held non-compliant, since it would not be clear whether the character(s) were meant to be deleted or not.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1, 12, and 17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 1 has a limitation stating "the value has at least three states to represent the at least two of the following relationships...". Claim 12 has a limitation stating "producing a result which has at least three states to indicate at least two of a following mathematical relationships...". Claim 17 has a limitation stating "determining an output operand which has at least three states indicative of the at least two mathematical relationships...". All of these limitations are essentially stating that the output of the comparison operation represents *two* of the mathematical relationships. However, the specification states that the output result represents only one of the mathematical relationships, i.e. represents the mathematical relationship that is true (Specification page 1, Table II). The specification has not described a way reasonable to one skilled in the art at the time the application was filed whether Applicant's invention had an output/result value presenting *two* mathematical relationships, not just one.

6. Claims 1, 12, and 17 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 1 has a limitation stating "the value has at least three states to represent the at least two of the following relationships...". Claim 12 has a limitation stating "producing a result which has at least three states to indicate at least two of a following mathematical relationships...". Claim 17 has a

limitation stating "determining an output operand which has at least three states indicative of the at least two mathematical relationships...". All of these limitations are essentially stating that the output of the comparison operation represents *two* of the mathematical relationships. However, the specification states that the output result represents only one of the mathematical relationships, i.e. represents the mathematical relationship that is true (Specification page 1, Table II). It is unclear how a single output value can represent two mathematical relationships.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 1 recites the limitation " the value has at least three states to represent the at least two of the following relationships..." in lines 12-13 of the claim. There is insufficient antecedent basis for this limitation in the claim.

9. Claim 12 recites the limitation " producing a result which has at least three states to indicate at least two of a following mathematical relationships..." in lines 8-9 of the claim. There is insufficient antecedent basis for this limitation in the claim.

10. Claim 17 recites the limitation "determining an output operand which has at least three states indicative of the at least two mathematical relationships..." in lines 7-8 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 1, 3, 5, 8-9, 11-14, 16-18, and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over John L. Hennessy and David A. Patterson's Computer Organization and Design: The Hardware/Software Interface Second Edition ©1998 (herein referred to as Hennessy) in view of Brian W. Kernighan and Dennis M. Ritchie's The C Programming Language ©1978 (herein referred to as Kernighan).

13. Referring to claim 1, Hennessy has taught a processing core that executes a compare instruction, the processing core comprising:

a. A plurality of general-purpose registers comprising a first input operand register, a second input operand register and an output operand register (Hennessy Pages 345, 347; 356-357; and 360);

b. A register file comprising the plurality of general-purpose registers (Hennessy Pages 345 and 360);

c. Comparison logic coupled to the register file (Hennessy pages 357 and 361),

d. Decode logic, which selects the output operand register from the plurality of general purpose registers (Hennessy Pages 345, 347; 356-357; and 360); and

e. A store path between the comparison logic and the selected output operand register, wherein the value is stored in the selected output operand register (Hennessy Pages 345, 347; 356-357; and 360).

14. Hennessy has not explicitly taught

i. The comparison logic tests for at least two of a following relationships with the compare instruction alone: less than, equal to, greater than or no valid relationship,

ii. The comparison logic with the compare instruction alone produces a value, and

iii. The value has at least three states to represent at least two of the following relationships: less than, equal to, greater than or no valid relationship.

15. However, Hennessy has taught that, in order to command a computer's hardware, then a language must be used and uses the C programming language as an example (Hennessy Pages 106-107, Section 3.1). Kernighan has taught

i. The comparison logic tests for at least two of a following relationships with the compare instruction alone: less than, equal to, greater than or no valid relationship (Kernighan Page 101 "strcmp"),

ii. The comparison logic with the compare instruction alone produces a value (Kernighan Page 101 "strcmp"), and

iii. The value has at least three states to represent at least two of the following relationships: less than, equal to, greater than or no valid relationship (Kernighan Page 101 "strcmp").

16. A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by Hennessy and Kernighan, that the computer hardware must be commanded to function (Hennessy Pages 106-107, Section 3.1) and that the C programming language is less restrictive and more generally applicable so it is more convenient and effective to use (Kernighan page ix). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the C programming language of

Kernighan in the device of Hennessy to control the hardware functions with a more convenient and effective language.

17. Referring to claim 3, Hennessy has taught wherein said decode logic selects the first and second input operand registers from the plurality of general-purpose registers (Hennessy Pages 345, 347; 356-357; and 360).

18. Referring to claim 5, Hennessy has taught:

a. A first load path between the first input operand register and the comparison logic (Hennessy Page 360); and

b. A second load path between the second input operand register and the comparison logic (Hennessy Page 360).

19. Referring to claim 8, Hennessy has not taught wherein the value is an integer. However, Hennessy has taught that, in order to command a computer's hardware, then a language must be used and uses the C programming language as an example (Hennessy Pages 106-107, Section 3.1). Kern has taught wherein the value is an integer (Kernighan Page 101 "strcmp"). A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by Hennessy and Kernighan, that the computer hardware must be commanded to function (Hennessy Pages 106-107, Section 3.1) and that the C programming language is less restrictive and more generally applicable so it is more convenient and effective to use (Kernighan page ix). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the C programming language of Kernighan in the device of Hennessy to control the hardware functions with a more convenient and effective language.

20. Referring to claim 9, Hennessy has taught

a. The first input operand register is a double precision floating point data type (Hennessy pages 276-277);

b. The second input operand register is a single precision floating point data type (Hennessy pages 276-277); and

c. The output operand register is a double precision floating point data type (Hennessy pages 276-277).

21. Referring to claim 11, Hennessy has taught wherein the register comprises special purpose registers which cannot store an output operand (Hennessy Page 360). In regards to Hennessy, the PC register does not receive an output operand from the ALU.

22. Referring to claim 12, Hennessy has taught a method for performing a compare operation, the method comprising steps of:

a. Decoding a compare instruction (Hennessy Pages 345, 347; 356-357; and 360);

b. Configuring first and second paths between a register file and comparison logic (Hennessy Pages 345, 347; 356-357; and 360);

c. Configuring a third path between the comparison logic and the register file (Hennessy Pages 345, 347; 356-357; and 360); and

d. Coupling the result to a general-purpose register in the register file (Hennessy Pages 345, 347; 356-357; and 360).

23. Hennessy has not taught comparing a first input operand and a second input operand with the compare operation alone, wherein the comparing step comprises step of:

a. Producing a result, which has at least three states to indicate at least two of a following mathematical relationships between the first input operand and the second input operand: less than, equal to, greater than, or no valid relationship.

24. However, Hennessy has taught that, in order to command a computer's hardware, then a language must be used and uses the C programming language as an example (Hennessy Pages 106-107, Section 3.1). Kernighan has taught comparing a first input operand and a second input operand with the compare operation alone (Kernighan Page 101 "strcmp"), wherein the comparing step comprises step of:

a. Producing a result, which has at least three states to indicate at least two of a following mathematical relationships between the first input operand and the second input operand: less than, equal to, greater than, or no valid relationship (Kernighan Page 101 "strcmp").

25. A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by Hennessy and Kernighan, that the computer hardware must be commanded to function (Hennessy Pages 106-107, Section 3.1) and that the C programming language is less restrictive and more generally applicable so it is more convenient and effective to use (Kernighan page ix). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the C programming language of Kernighan in the device of Hennessy to control the hardware functions with a more convenient and effective language.

26. Referring to claim 13, Hennessy has taught a step of enabling the comparison logic in an arithmetic logic unit (Hennessy Pages 345, 347; 356-357; and 360).

27. Referring to claim 14, Hennessy has taught wherein the configuring steps each comprise a step of addressing a general-purpose register in the register file (Hennessy Pages 345, 347; 356-357; and 360).

28. Referring to claim 16, Hennessy has not explicitly taught wherein the comparing step comprises a step of converting a data type of at least one of the first or second input operands. However, Hennessy has taught that, in order to command a computer's hardware, then a language must be used and uses the C programming language as an example (Hennessy Pages 106-107, Section 3.1). Kern has taught wherein the value is an integer (Kernighan Page 101 "strcmp"). A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by Hennessy and Kernighan, that the computer hardware must be commanded to function (Hennessy Pages 106-107, Section 3.1) and that the C programming language is less restrictive and more generally applicable so it is more convenient and effective to use (Kernighan page ix). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the C programming language of Kernighan in the device of Hennessy to control the hardware functions with a more convenient and effective language.

29. Referring to claim 17, Hennessy has taught a method for executing a compare instruction in a processor, the method comprising steps of:

a. Issuing the compare instruction (Hennessy Pages 345, 347; 356-357; and 360);

b. Storing the output operand in a general-purpose register of a register file (Hennessy Pages 345, 347; 356-357; and 360).

30. Hennessy has not taught

a. Comparing a first input operand and a second input operand to determine at least two mathematical relationships between the first and second input operands, wherein the compare instruction alone causes the comparing step;

b. Determining an output operand which has at least three states indicative of the at least two mathematical relationships; and

c. Wherein the output operand alone indicates the at least two mathematical relationships between the first and second input operands.

31. However, Hennessy has taught that, in order to command a computer's hardware, then a language must be used and uses the C programming language as an example (Hennessy Pages 106-107, Section 3.1). Kern has taught

a: Comparing a first input operand and a second input operand to determine at least two mathematical relationships between the first and second input operands, wherein the compare instruction alone causes the comparing step (Kernighan Page 101 "strcmp");

b. Determining an output operand which has at least three states indicative of the at least two mathematical relationships (Kernighan Page 101 "strcmp"); and

c. Wherein the output operand alone indicates the at least two mathematical relationships between the first and second input operands (Kernighan Page 101 "strcmp").

32. A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by Hennessy and Kernighan, that the computer hardware must be commanded to function (Hennessy Pages 106-107, Section 3.1) and that the C programming

language is less restrictive and more generally applicable so it is more convenient and effective to use (Kernighan page ix). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the C programming language of Kernighan in the device of Hennessy to control the hardware functions with a more convenient and effective language.

33. Referring to claim 18, Hennessy has not taught wherein the comparing step comprises at least two of the following steps:

a. Determining if the first input operand is less than the second input operand;

b. Determining if the first input operand is greater than the second input operand;

c. Determining if the first input operand is equal to the second input operand; or

d. Determining if there is no valid relationship between the first input operand and the second input operand.

34. However, Hennessy has taught that, in order to command a computer's hardware, then a language must be used and uses the C programming language as an example (Hennessy Pages 106-107, Section 3.1). Kern has taught

a. Determining if the first input operand is less than the second input operand (Kernighan Page 101 "strcmp");

b. Determining if the first input operand is greater than the second input operand (Kernighan Page 101 "strcmp");

c. Determining if the first input operand is equal to the second input operand (Kernighan Page 101 "strcmp"); or

d. Determining if there is no valid relationship between the first input operand and the second input operand (Kernighan Page 101 "strcmp").

35. A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by Hennessy and Kernighan, that the computer hardware must be commanded to function (Hennessy Pages 106-107, Section 3.1) and that the C programming language is less restrictive and more generally applicable so it is more convenient and effective to use (Kernighan page ix). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the C programming language of Kernighan in the device of Hennessy to control the hardware functions with a more convenient and effective language.

36. Referring to claim 20, Hennessy has taught wherein the general-purpose register is used to store operators from other types of instructions (Hennessy Pages 345, 347; 356-357; and 360).

37. Referring to claim 21, Hennessy has taught wherein the value in the operand register can be written to a location outside of the processing core (Hennessy Pages 345, 347; 356-357; and 360).

38. Referring to claim 22, Hennessy has taught wherein the result can be written to a location outside of the processing core (Hennessy Pages 345, 347; 356-357; and 360).

39. Claims 2, 4, 10, 15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over John L. Hennessy and David A. Patterson's <u>Computer Organization and Design: The Hardware/Software Interface</u> Second Edition ©1998 (herein referred to as Hennessy) in view of Brian W. Kernighan and Dennis M. Ritchie's <u>The C Programming Language</u> ©1978 (herein

referred to as Kernighan), as applied to claim 1 above, and further in view of Colwell et al., U.S. Patent No. 4,833,599 (herein referred to as Colwell).

40. Regarding claim 2, Alpha has taught the processing core that executes the compare instruction as set forth in claim 1, but has not explicitly taught wherein a very long instruction word includes a plurality of compare instructions.

41. However, Colwell has taught a processor that executes multiple conditional branch instructions that reside in a VLIW instruction in parallel to improve execution speed and reduce the delay associated with branch mis-predictions (Colwell Col.1 line 40 – Col.2 line 18 and Col.3 lines 3-34). One of ordinary skill in the art would have recognized that it is desirable and a goal of microprocessor design to improve the speed and throughput of a microprocessor. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of the Alpha to process a plurality of conditional branch instructions in a VLIW instruction in parallel to improve the execution speed of the processor.

42. Regarding claim 4, Alpha has taught the processing core that executes the compare instruction as set forth in claim 1, but has not explicitly taught wherein the processing core issues a plurality of compare instructions at one time.

43. However, Colwell has taught a processor that executes multiple conditional branch instructions that reside in a VLIW instruction in parallel to improve execution speed and reduce the delay associated with branch mis-predictions (Colwell Col.1 line 40 – Col.2 line 18 and Col.3 lines 3-34). It is inherent to the parallel execution of multiple instructions then is the parallel issue of multiple instructions. One of ordinary skill in the art would have recognized that it is desirable and a goal of microprocessor design to improve the speed and throughput of a

microprocessor, and one method of doing so is to increase the instruction-level parallelism by issuing and subsequently executing multiple instructions in parallel (Colwell Col.1 lines 12-26). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of the Alpha to issue a plurality of compare instructions at one time so they can be executed in parallel and thus increase the throughput and execution speed of the processor.

44. Regarding claim 10, Alpha has taught the processing core that executes the compare instruction as set forth in claim 1, but has not explicitly taught wherein the processing core further comprises a plurality of processing paths that are coupled to the register file.

45. However, Colwell has taught a processor with multiple processor clusters, each containing multiple processing paths (integer and floating point processors) with each processing path connecting to a register file (Colwell Col.5 lines 47-55), so that multiple instructions can be executed in parallel each cycle, providing an increase in processor performance (Colwell Col.1 lines 7-26). One of ordinary skill in the art would have recognized that it is desirable and a goal of microprocessor design to improve the speed and throughput of a microprocessor. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of the Alpha to process a plurality of conditional branch instructions in a VLIW instruction in parallel to improve the execution speed of the processor.

46. Regarding claim 15, Alpha has taught the method for performing the compare operation as set forth in claim 12, but has not explicitly taught wherein a compare operation is comprised within a very long instruction word.

47. However, Colwell has taught a processor that executes multiple conditional branch instructions that reside in a VLIW instruction in parallel to improve execution speed and reduce

the delay associated with branch mis-predictions (Colwell Col.1 line 40 – Col.2 line 18 and Col.3 lines 3-34). One of ordinary skill in the art would have recognized that it is desirable and a goal of microprocessor design to improve the speed and throughput of a microprocessor. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of the Alpha to process a plurality of conditional branch instructions in a VLIW instruction in parallel to improve the execution speed of the processor.

48. Regarding claim 19, Alpha has taught the method for executing the compare instruction in the processor as set forth in claim 17, but has not explicitly taught wherein the compare instruction is a very long instruction word which comprises a plurality of compare instructions which are processed in parallel down separate processing paths.

49. However, Colwell has taught a processor that executes multiple conditional branch instructions that reside in a VLIW instruction in parallel to improve execution speed and reduce the delay associated with branch mis-predictions (Colwell Col.1 line 40 – Col.2 line 18 and Col.3 lines 3-34). One of ordinary skill in the art would have recognized that it is desirable and a goal of microprocessor design to improve the speed and throughput of a microprocessor. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of the Alpha to process a plurality of conditional branch instructions in a VLIW instruction in parallel to improve the execution speed of the processor.

Response to Arguments

50. Applicant's arguments with respect to claims 1-5 and 8-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

51. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

52. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

53. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

54. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

55. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
29 June 2005

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SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100